Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

Claims 1-93 (canceled)

94. (currently amended) ~~An electronic component~~ A semiconductor chip or wafer comprising:

a silicon ~~semiconductor~~ substrate ~~having multiple semiconductor devices~~;

a first ~~an interconnecting~~ metallization structure over said silicon ~~semiconductor~~ substrate;

a passivation ~~an insulating~~ layer over said ~~interconnecting~~ first metallization structure; and

a second ~~an upper~~ metallization structure over said passivation ~~insulating~~ layer, wherein said second ~~upper~~ metallization structure comprises a gold ~~metal~~ layer having a thickness of between 2 and 100 μm, and wherein said second ~~upper~~ metallization structure connects multiple separate portions of said first ~~interconnecting~~ metallization structure.

95. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 94, wherein said passivation ~~insulating~~ layer comprises a topmost nitride layer of said semiconductor chip or wafer.

96. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 94, wherein said ~~insulating layer comprises a~~ passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

97. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 94, wherein said passivation ~~insulating~~ layer comprises a topmost CVD-formed layer of said semiconductor chip or wafer.

98. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 94, wherein said ~~interconnecting~~ first metallization structure comprises a first contact pad exposed by an opening in said passivation ~~insulating~~ layer, and said second ~~upper~~ metallization structure comprises a second contact pad connected to said first contact pad, wherein the positions of said first and second contact pads from a top view are different.

99. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 94, wherein said second metallization structure further comprises a metal layer under said gold layer, wherein said metal layer comprises titanium. ~~metal layer comprises gold.~~

100. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 94 ~~99~~, wherein said second ~~upper~~ metallization structure further comprises ~~an underlying~~ a metal layer under said gold ~~metal~~ layer, wherein said ~~underlying~~ metal layer comprises ~~titanium~~ tungsten.

101. (canceled)

102. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 94 further comprising a topmost polymer layer over said ~~insulating~~ passivation layer, wherein said second ~~upper~~ metallization structure is over said topmost polymer layer.

103-104. (canceled)

105. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 94, wherein said gold ~~metal~~ layer is electroplated.

106. (currently amended) A semiconductor chip or wafer ~~An electronic component~~ comprising:

a silicon ~~semiconductor~~ substrate ~~having multiple semiconductor devices~~;

a first ~~an interconnecting~~ metallization structure over said ~~semiconductor~~ silicon substrate, wherein said first metallization structure ~~and comprising~~ comprises a first contact pad;

a passivation ~~an insulating~~ layer over said ~~interconnecting~~ first metallization

structure, wherein an opening in said passivation layer exposes said first contact pad ~~is exposed by an opening in said insulating layer~~; and

a second ~~an upper~~ metallization structure over said passivation ~~insulating~~ layer, wherein said second metallization structure ~~and comprising~~ comprises a gold layer with a thickness of between 2 and 100 μm, wherein said ~~upper~~ second metallization structure comprises a second contact pad connected to said first contact pad, and wherein the positions of said first and second contact pads from a top view are different.

107. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 106, wherein said passivation ~~insulating~~ layer comprises a topmost nitride layer of said semiconductor chip or wafer.

108. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 106, wherein said ~~insulating layer comprises a~~ passivation layer comprises a topmost oxide layer of said semiconductor chip or wafer.

109. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 106, wherein said passivation ~~insulating~~ layer comprises a topmost CVD-formed layer of said semiconductor chip or wafer.

110. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 106, wherein said second ~~upper~~ metallization structure further comprises a metal layer under said gold layer, wherein said metal layer comprises titanium tungsten.

111. (canceled)

112. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 106, wherein said second contact pad is used to be wirebonded thereto.

113. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 106 further comprising a wirebond on ~~connected to~~ said second contact pad.

114. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 106 further comprising a metal bump on said second contact pad.

115. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 106 further comprising a solder bump on said second contact pad..

116. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 106 further comprising a topmost polymer layer over said passivation ~~insulating~~ layer, wherein said gold layer is ~~upper metallization structure comprises an upper metal layer~~ over said topmost polymer layer.

117-118. (canceled)

119. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 106, wherein said gold layer is electroplated.

120. (currently amended) A semiconductor chip or wafer ~~An electronic component~~ comprising:

a silicon ~~semiconductor~~ substrate ~~having multiple semiconductor devices~~;

a first ~~an interconnecting~~ metallization structure over said silicon ~~semiconductor~~ substrate, wherein said first metallization structure comprises a first contact pad; ~~and comprising a contact point;~~

a passivation layer over said first ~~interconnecting~~ metallization structure, wherein an opening in said passivation layer exposes said first contact pad; and ~~point is exposed by an opening in said passivation layer; and~~

a second contact pad connected to said first contact pad, ~~point,~~ wherein said second contact pad comprises a gold layer with a thickness of between 2 and 100 μm and is used to be wirebonded thereto.

121-122. (canceled)

123. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 120 further comprising a polymer layer over said passivation layer, wherein said second contact pad is over said polymer layer.

124-125. (canceled)

126. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 120, wherein said passivation ~~insulating~~ layer comprises a topmost nitride layer of said semiconductor chip or wafer.

127. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 120, wherein said passivation ~~insulating~~ layer comprises a topmost oxide layer of said semiconductor chip or wafer.

128. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 120, wherein said passivation layer comprises a topmost CVD-formed layer of said semiconductor chip or wafer.

129. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 120, wherein said gold layer is electroplated.

130. (canceled)

131. (currently amended) The semiconductor chip or wafer ~~electronic component~~ of claim 120 further comprising a wirebond on ~~connected to~~ said second contact pad.

132-135. (canceled)